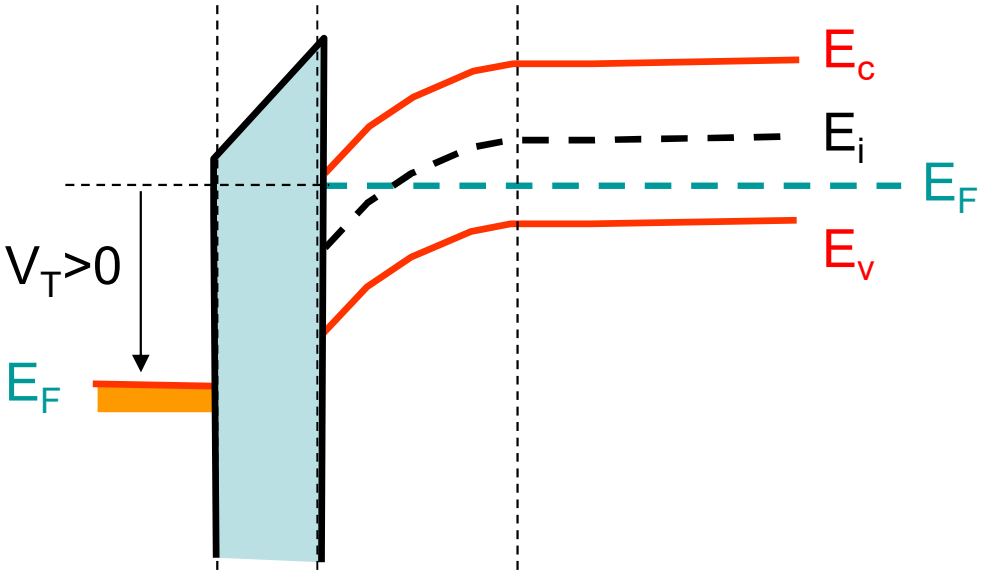
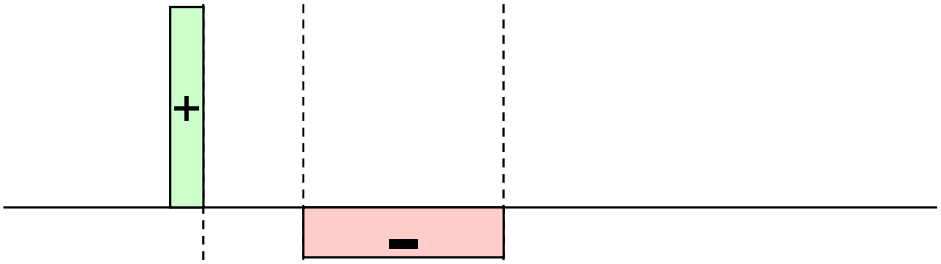
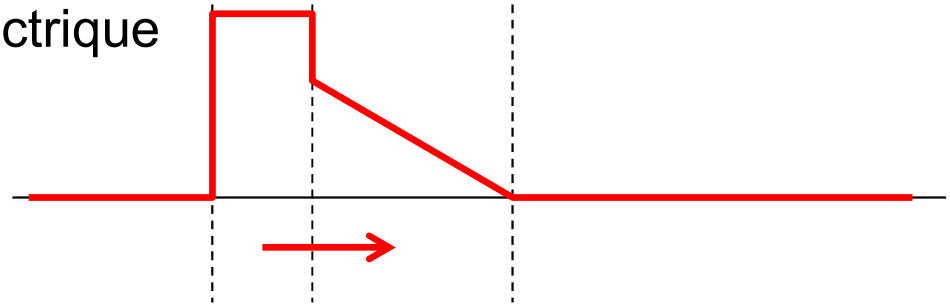
Bandes



Charges



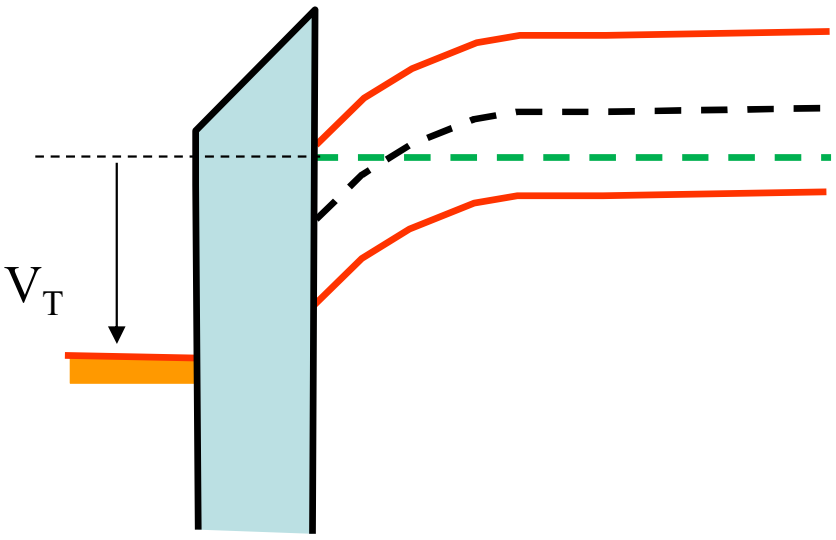
Champ électrique



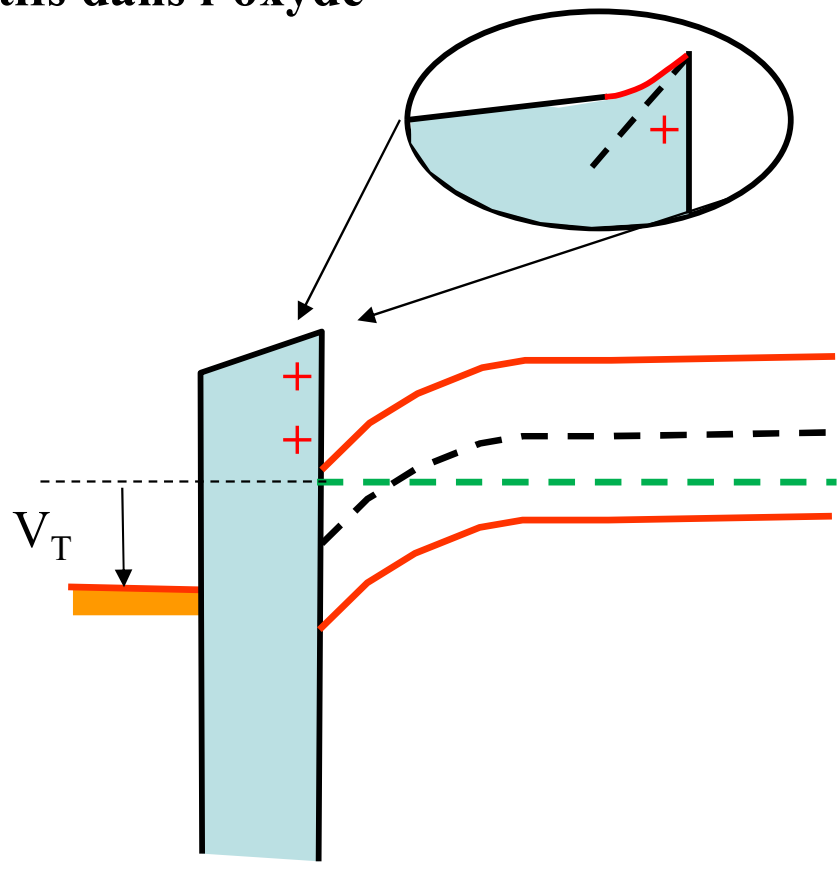
Après introduction de charges fixes positives à l'interface:

	Augmente	Diminue	Reste fixe
Potentiel de surface ψ_S			X
Charges d'espace dans la zone de déplétion			X
Champ électrique dans l'oxyde		X	
Charges dans le métal		X	
Tension électrique sur le métal (Tension de threshold V_T)		X	

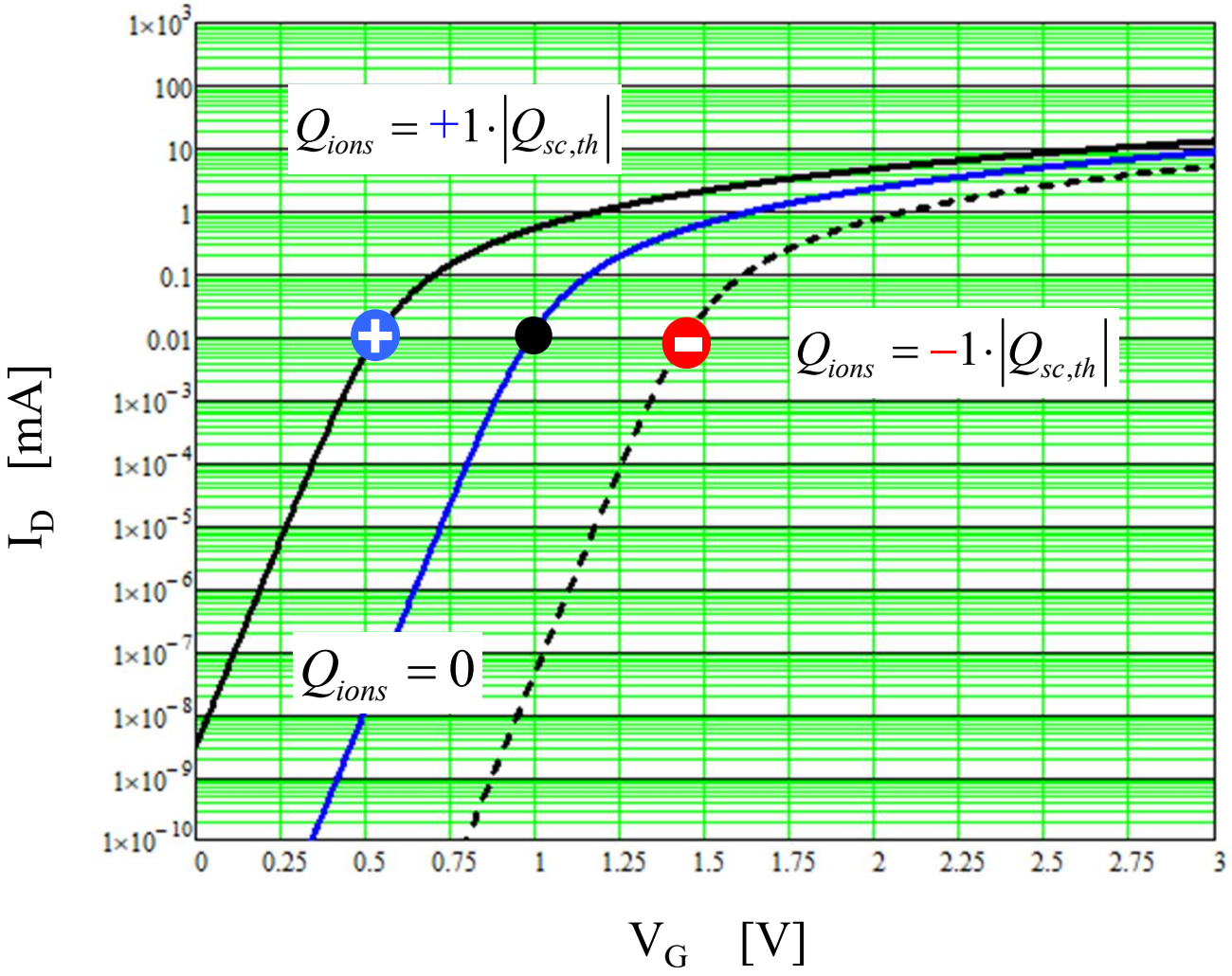
Situation de depart sans ion dans l'oxyde



Ions positifs dans l'oxyde



Réduction du threshold



$N_A = 10^{17}$ cm^{-3}

$\varepsilon_{ox} = 4$

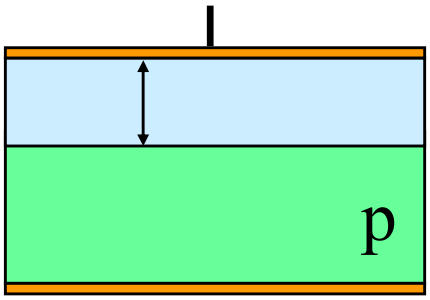
$d_{ox} = 10$ nm

$$|Q_{sc,th}| = 1.6 \cdot 10^{-15} \left[C / um^2 \right]$$

$n = 1.27$ dans les trois cas

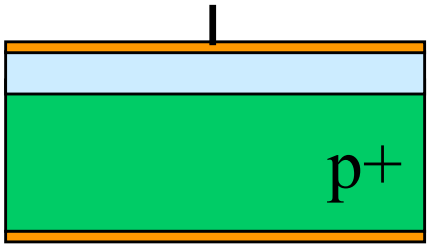
$$V_T = V_{T0} - \frac{Q_{ion}}{C_{ox}}$$

Field Oxide



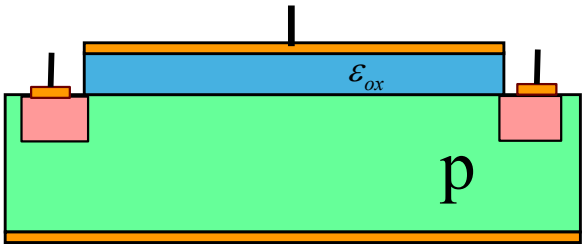
d_{ox} ↗ V_T ↗

Chanel stop



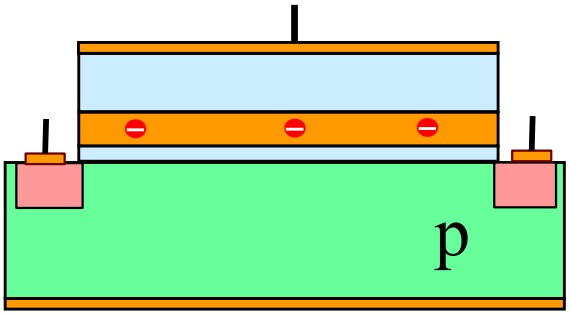
p ↗ V_T ↗

High K



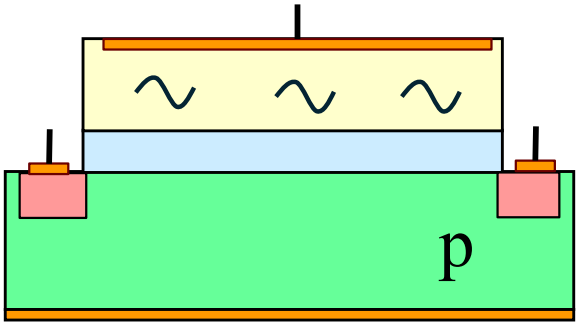
ε_{ox} ↗ V_T ↘

Floatging gate memory



⊖⊖ ↗ V_T ↗

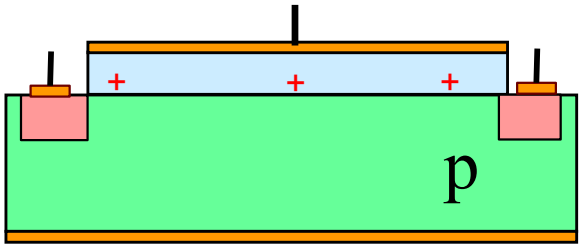
ISFET



∼ − V_T ↗

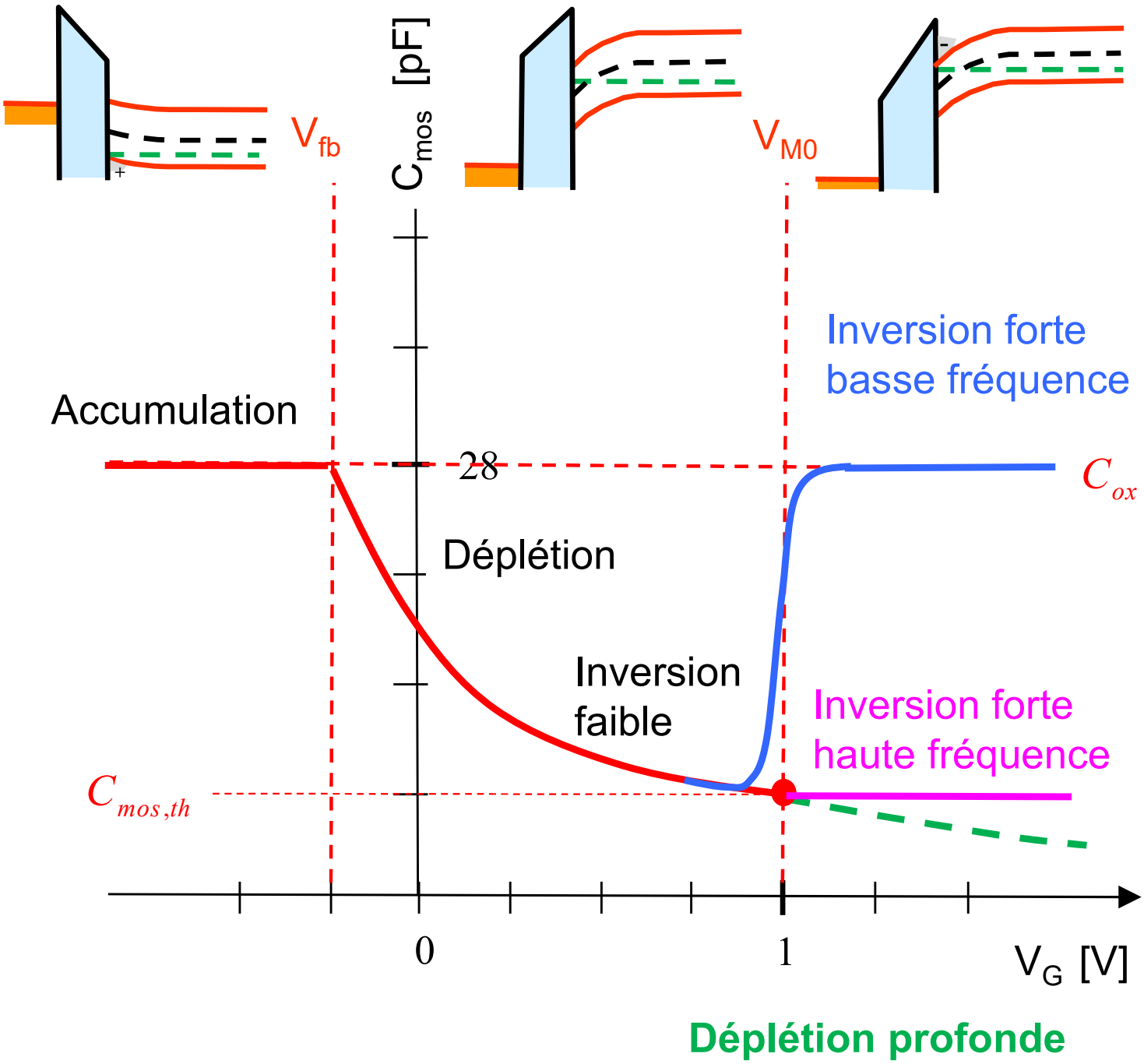
∼ + V_T ↘

Ion implant



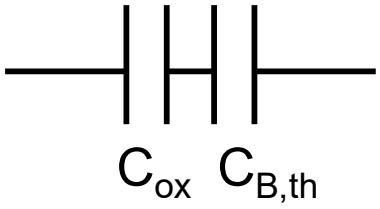
\+ V_T ↘

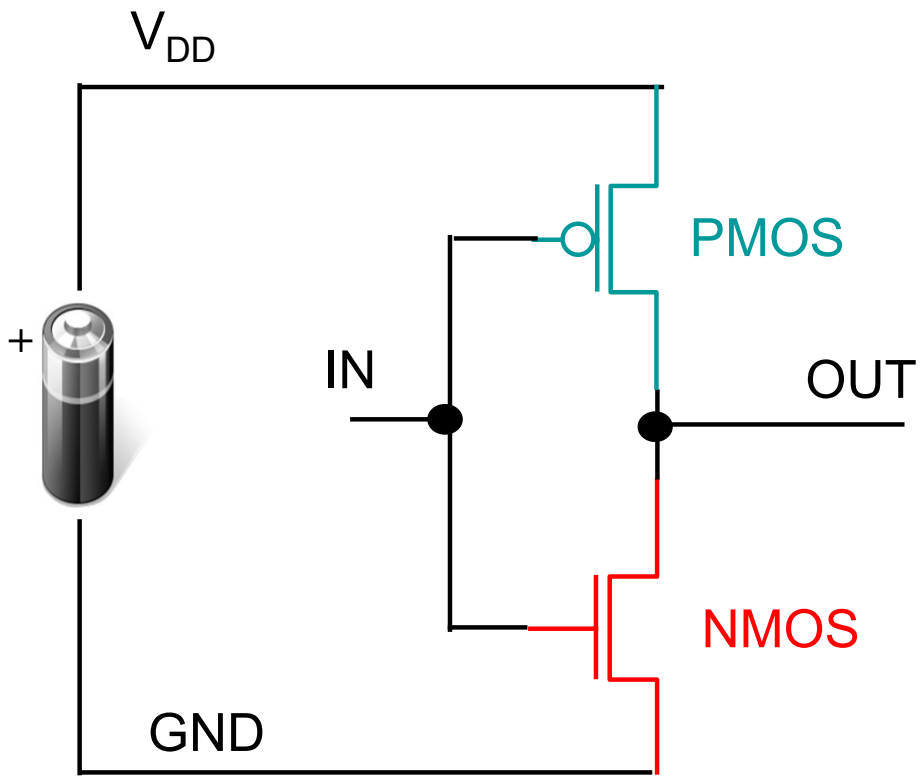
− V_T ↗

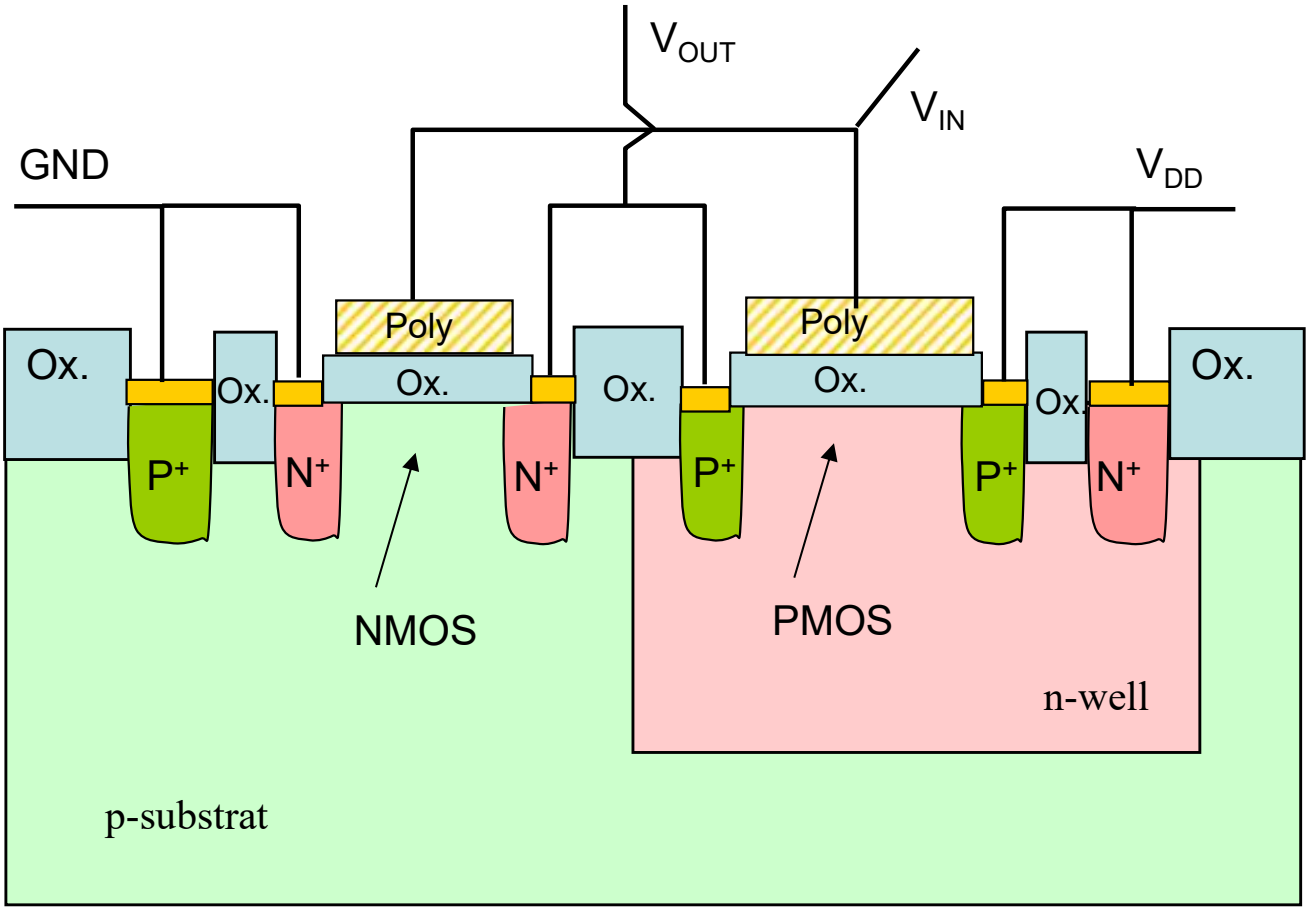


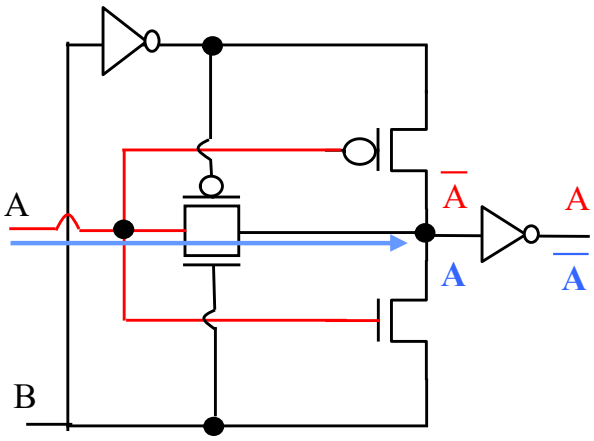
$$C_{mos,th} = \frac{C_{ox} \cdot C_{B.th}}{C_{ox} + C_{B,th}} = C_{ox} \cdot \frac{C_{B,th}/C_{ox}}{1 + C_{B,th}/C_{ox}}$$

$$C_{mos,th} = C_{ox} \cdot \frac{n-1}{n} = 7\,[pF]$$




V_{DD}
+
PMOS
IN
OUT
NMOS
GND


V_{OUT}
V_{IN}
GND
V_{DD}
Poly
Poly
Ox.
Ox.
Ox.
Ox.
Ox.
Ox.
Ox.
P^+
N^+
N^+
P^+
P^+
N^+
NMOS
PMOS
n-well
p-substrat



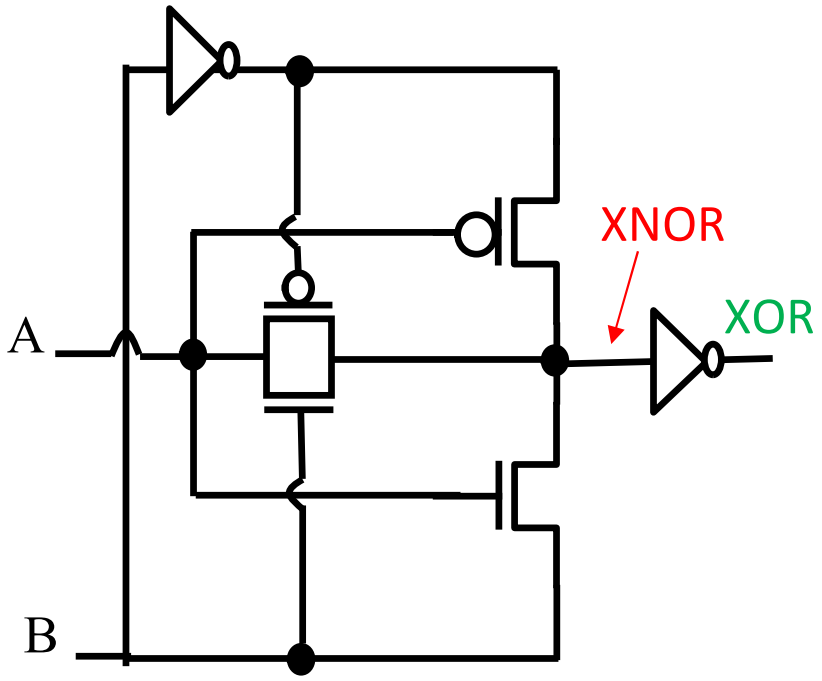
XOR avec 8 transistors

(voir script)

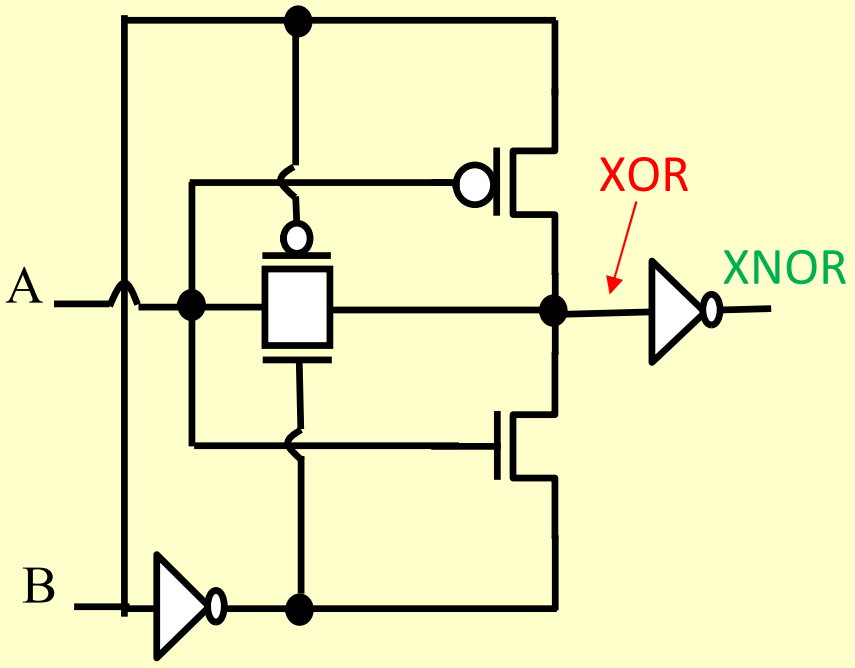
L'inverseur final sert à isoler la sortie de l'entrée !

A	B		OUT
0	0	**1**	**0**
1	0	**0**	**1**
0	1	**0**	**1**
1	1	**1**	**0**

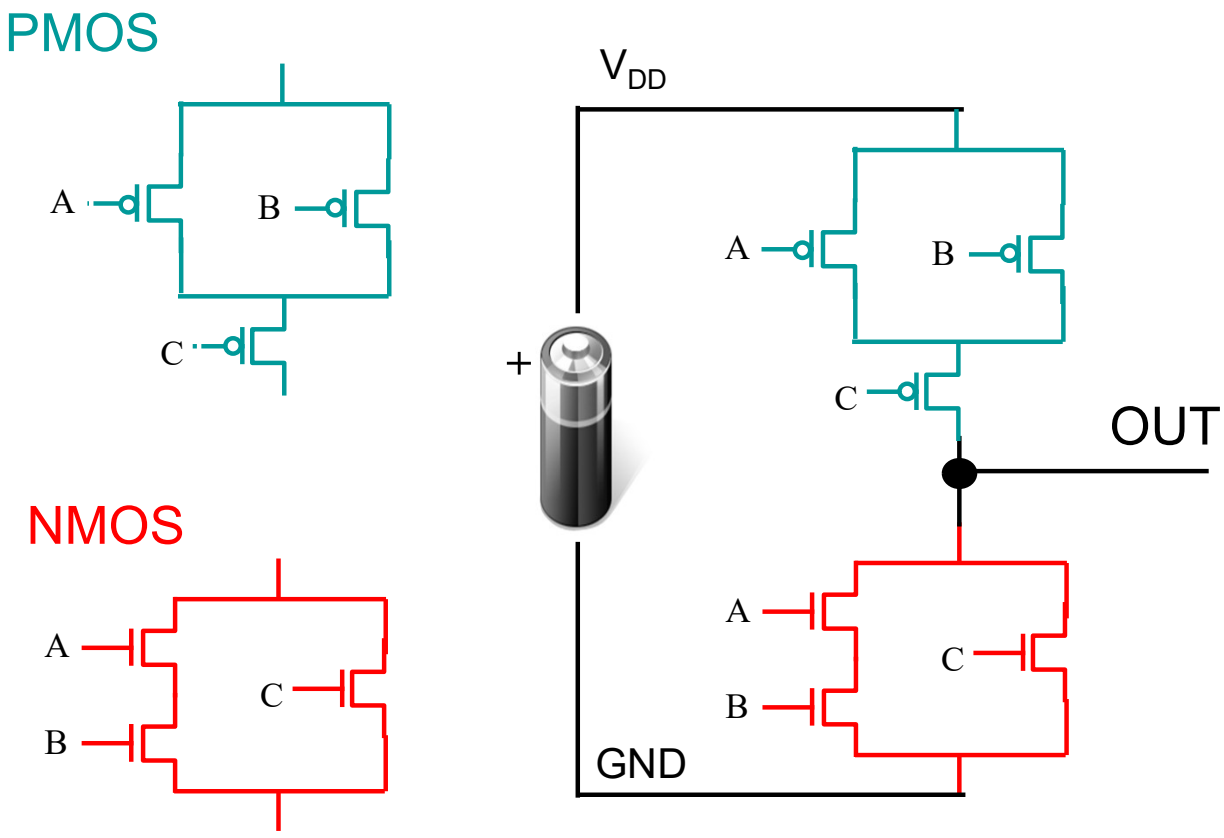
XNOR XOR



XOR: 8 transistors et isolation
XNOR: 6 transistors sans isolation



XNOR: 8 transistors et isolation
XOR: 6 transistors sans isolation



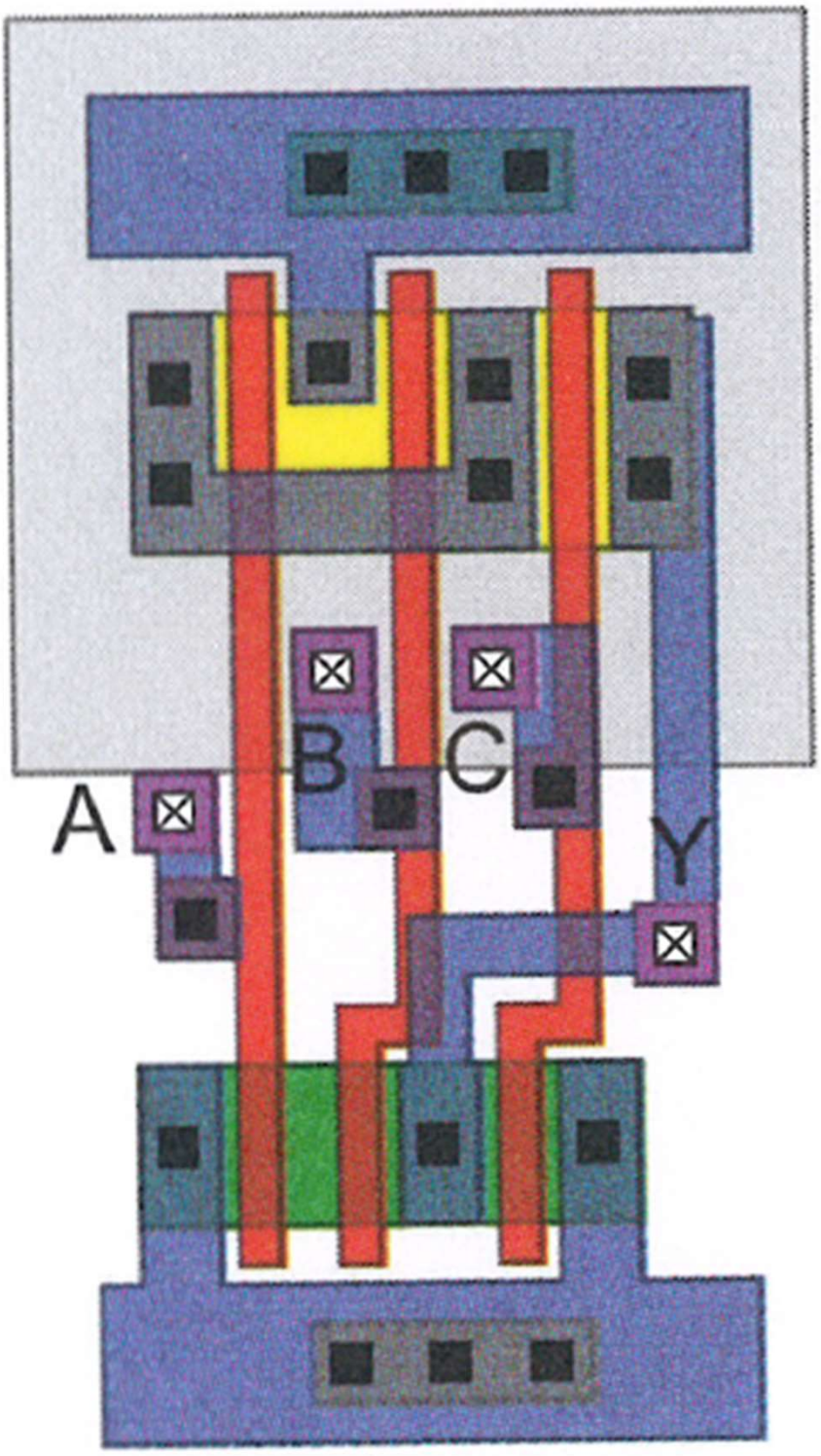
(voir script) AOI-21 → $\overline{[(A \text{ et } B) \text{ ou } C]}$

And-Or-Invert

	A	B	C	AOI-21
	0	0	0	1
	0	0	1	0
	0	1	0	1
OR	0	1	1	0
	1	0	0	1
	1	0	1	0
	1	1	0	0
AND	1	1	1	0

Layout AOI-21

«And-Or-Invert»



Weste/Harris, « CMOS VLSI design », Addison-Wesley